Appendix C: Registers

(a) Interrupt Capture Register (C0000)

Bit	Interrupt	Level	Source
D7	V-DRIVE	7	leading edge of VFB
D6	DPB-I	6	Deflection Processor Board (DPB)
D5	IOP-I	5	I/O Processor (IOP)
D4	ACON-I	4	ACON processor
D3	TIMER	3	timer (from IOP)

Notes: 1) Interrupts with smaller levels have lower priority.
2) Writing a binary 1 to a bit clears the associated interrupt. Writing a binary 0 to a bit has no effect.

(b) Interrupt Status Register (C8000)

Bit	Signal	Description
0	DPB-WR	DPB write
1	DPB-RD	DPB read
2	IOP-WR	IOP write
3	IOP-RD	IOP read
4	ACON-WR	ACON write
5	ACON-RD	ACON read
6	n/a	reserved - tied low
7	n/a	reserved - tied low

Notes: 1) A high "write" input indicates unread data from the device.
2) A high "read" input indicates that the device has read the last byte sent to it.

(c) Display Register (EC000)

Bit	Function
D8	Text display bit (high = text on)
D9	Background mode - bit 0
D10	Background mode - bit 1
D11	Background mode - bit 2
D12	unused
D13	Crosshatch line width - bit 0
D14	Crosshatch line width - bit 1
D15	Crosshatch line width - bit 2

Background Display Modes:

D11	D10	D9	Mode
0	0	0	Dense crosshatch
0	0	1	Crosshatch
0	1	0	Dot field
0	1	1	Crosshatch with dots
1	0	0	White field
1	0	1	Grayscale
1	1	0	External video
1	1	1	Black field

Crosshatch Line Width:

D15	D14	D13	Delay (ns)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	15
1	0	0	20
1	0	1	25
1	1	0	30
1	1	1	30